Communication Processor ATM Firmware

Piotr Lavrov <lvr@oktetlabs.ru>

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Project dates: May 2000 – December 2001

Manpower: 120 man-months

Team Leader: Victor Vengerov, Senior Software Engineer

The task was to develop and test the firmware code for communication processor handling all ATM-related functionality. The project included:

- the study of the similar communication processors, including ATMizer, Power QUICC II, other;
- review of related standards;
- definition of features to be implemented in the firmware (see feature list below);
- design of firmware architecture and data structures;
- development of firmware functional model in ANSI C;
- development of host driver prototype;
- development of test suite to verify the functionality;
- clarification of chip’s hardware architecture;
- development of target hardware simulator (including communication processor ISS, controllers and data path models)
- conversion of the C model into proprietary assembler language;
- testing the firmware on the simulator and improvement of test coverage;
- development of performance tests; evaluation of firmware performance using the simulator;
- development of firmware code optimization tools;
- additional manual code optimization to fit into size and performance requirements,
- verification of the code on the Verilog model of the processor;
- testing the functionality on the real silicon;
- creation the "ATM Firmware User’s Manual" document draft.

The project has been completed in time. Defined functionality has been implemented in firmware completely. Firmware tests were run on actual hardware successfully.

Firmware fit into 8K instruction words; on project completion about 200 instruction words were reserved for maintenance. ADSL performance objective was achieved. VDSL performance achieved with restrictions (descriptors stored in the local memory).

1. Firmware Features

The basic feature list of the developed firmware includes:

- UTOPIA Level 2 Master interface; up to 31 PHYs supported
  - FIFO full and periodical timer transmit rate modes
- Supports up to 256 connection descriptors in local memory; up to 8K connection descriptors in external memory.
- No restrictions on buffer alignment;
- Buffer management;
- AAL0
  - switch mode
  - optional CRC10 insertion/check
- AAL1
  - configurable support of partially-filled cells
  - configurable support for structured data transfer;
  - structured pointer synchronization;
  - sequence number check;
  - lost/misinserted cells detection; dummy cells insertion;
  - SRTS generation, clock recovery.
- AAL2
  - CPCS (as per ITU-T I.363.2) implemented in firmware
  - support for different asynchronous data sources (e.g. DSP)
  - Optional Combined Use timer support;
- AAL5
- ATM Forum Traffic Management 4.1 support:

    - CBR, UBR, VBR (type 1, 2), GFR traffic types
    - UBR+ (UBR with minimum desired cell rate specified) support
    - ABR support, resource management cells handled in firmware
    - Static (CBR-only) and dynamic scheduling algorithms implemented
- ITU-T I.610 (02/99) OAM
    - F4 and F5 flow support
    - I.610 Performance Monitoring implemented in firmware
    - In-band OAM cell transmission
- Statistics gathering

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